UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,554	12/20/2001	Linda J. Rankin	10559-637001/P12341	4687

20985 7590 01/24/2005

FISH & RICHARDSON, PC
12390 EL CAMINO REAL
SAN DIEGO, CA 92130-2081

EXAMINER	
AUVE, GLENN ALLEN	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 01/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/029,554	RANKIN ET AL.	
	Examiner	Art Unit	
	Glenn A. Auve	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-13,15-28 and 30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-8,10-13,15-17,19-28 and 30* is/are rejected.

7)☒ Claim(s) *9 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3,5-8,12,13,15-17,20-28, and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Oi et al., U.S. Pat. Application Publication No. 2003/0007493 A1 (previously cited).

The Oi et al. (Oi) reference claims priority to a provisional application with a filing date of June 28, 2001. The provisional application contains the same specification and drawings as the application publication.

As per claim 1, Oi shows a method comprising: incorporating a multi-port switch into a multi-node computer system; and assigning at least a first port of the multi-port switch to a first domain of the nodes; assigning at least a second port of the multi-port switch to a second domain of the nodes, the first domain of the nodes and second domain of the nodes having separate and independent memory structures (figs. 1A and 1B and paragraph [0016], wherein the system has at least two domains, each with its own address space; each domain containing a collection of nodes coupled to routers for communication).

As for claim 2, the argument for claim 1 applies. Oi also shows delivering transactions that are received by the multi-port switch and are identified as associated with the first domain, to the at least a first or more ports assigned to the first domain (paragraphs [0008] and [0016-

0022]).

As for claim 3, the argument for claim 1 applies. Oi also shows connecting nodes associated with the first domain to the at least a first port assigned to the first domain (fig.1B and paragraphs [0016-0022]).

As for claim 5, the argument for claim 1 applies. Oi also shows delivering transactions, which are received by the multi-port switch and are identified as associated with the second domain, to the at least a second or more ports assigned to the second domain (paragraphs [0008] and [0016-0022]).

As for claim 6, the argument for claim 1 applies. Oi also shows connecting nodes associated with the second domain to ports assigned to that second domain (fig.1B and paragraphs [0016-0022]).

As for claim 7, the argument for claim 1 applies. Oi also shows assigning at least a third port of the multi-port switch to a third domain; and connecting nodes associated with the third domain to ports assigned to that third domain (fig.1A shows that there can be any number of domains which would operate the same as the other domains).

As for claim 8, the argument for claim 7 applies. Oi also shows delivering transactions, which are received by the multi-port switch and specify the third domain, to the at least a third or more ports assigned to the third domain (fig.1B and paragraphs [0016-0022]).

As per claim 12, Oi shows a domain partitioning process for creating multiple domains in a multi-node computer system comprising: a first domain port assignment process for assigning at least a first port of said multi-port switch to a first domain; and a second domain port assignment process for assigning at least a second port of said multi-port switch to a second domain of the nodes, the first domain of the nodes and second domain of the nodes having separate and independent memory structures (figs. 1A and 1B and paragraph [0016], wherein

the system has at least two domains, each with its own address space; each domain containing a collection of nodes coupled to routers for communication).

As for claim 13, the argument for claim 12 applies. Oi also shows a first domain transaction routing process for routing transactions, which are received by said multi-port switch and specify the first domain, to one or more ports assigned to the first domain (paragraphs [0008] and [0016-0022]).

As for claim 15, the argument for claim 12 applies. Oi also shows a second domain transaction routing process for routing transactions, which are received by the multi-port switch and specify the second domain, to one or more ports assigned to the second domain (paragraphs [0008] and [0016-0022]).

As for claim 16, the argument for claim 12 applies. Oi also shows a third domain port assignment process for assigning at least a third port of the multi-port switch to a third domain (fig.1A shows that there can be any number of domains which would operate the same as the other domains).

As for claim 17, the argument for claim 16 applies. Oi also shows a third domain transaction routing process for routing transactions, which are received by the multi-port switch and specify the third domain, to one or more ports assigned to the third domain (fig.1A shows that there can be any number of domains which would operate the same as the other domains).

As per claim 20, Oi shows a domain partitioning process for creating multiple domains in a multi-node computer system that includes a multi-port switch containing a plurality of ports, the process comprising: a port assignment process for assigning at least a first port of said multi-port switch to a first one of a plurality of domains; and a second port assignment process for assigning at least a second port of the multi-port switch to a second one of the plurality of domains, the first one of the plurality of domains and the second one of the plurality of domains

having separate and independent memory structures (figs. 1A and 1B and paragraph [0016], wherein the system has at least two domains, each with its own address space; each domain containing a collection of nodes coupled to routers for communication).

As for claim 21, the argument for claim 20 applies. Oi also shows a transaction routing process for routing domain-specific transactions received by said multi-port switch to one or more ports assigned to the specified domain (paragraphs [0008] and [0016-0022]).

As per claim 22, Oi shows a computer program product residing on a computer readable medium having a plurality of instructions stored thereon which, when executed by the processor, cause that processor to: assign at least a first port of a multi-port switch to a first domain; assign at least a second port of the multi-port switch to a second domain, the first domain and the second domain having separate and independent memory structures; and route transactions, which are received by the multi-port switch and specify the first domain, to one or more ports assigned to the first domain (figs. 1A and 1B and paragraph [0016], wherein the system has at least two domains, each with its own address space; each domain containing a collection of nodes coupled to routers for communication).

As for claim 23, the argument for claim 22 applies. Oi also shows that said computer readable medium is a read-only memory (paragraph [0016]).

As for claim 24, the argument for claim 22 applies. Oi also shows that said computer readable medium is a hard disk drive (paragraph [0016]).

As per claim 25, Oi shows a processor and memory configured to: assign at least a first port of a multi-port switch to a first domain; assign at least a second port of the multi-port switch to a second domain, the first domain and the second domain having separate and independent memory structures; and route transactions, which are received by the multi-port switch and specify the first domain, to one or more ports assigned to the first domain (figs. 1A and 1B and

paragraph [0016], wherein the system has at least two domains, each with its own address space; each domain containing a collection of nodes coupled to routers for communication).

As for claim 26, the argument for claim 25 applies. Oi also shows that said processor and memory are incorporated into a network server (paragraphs [0003-0005]).

As for claim 27, the argument for claim 25 applies. Oi also shows that said processor and memory are incorporated into a workstation (paragraphs [0003-0005]).

As per claim 28, Oi shows a domain partitioning system comprising: a multi-port switch containing a plurality of ports (figs. 1A and 1B); a IO hub controller connected to one of said ports (120); a scalable node controller connected to one of said ports (110); and at least one microprocessor connected to said scalable node controller (in node 110); wherein the domain partitioning system is configured to include a first domain port assignment process for assigning at least a first port of said multi-port switch to a first domain; the domain partitioning system is configured to include a second domain port assignment process for assigning at least a second port of said multi-port switch to a second domain of the nodes, the first domain and the second domain having separate and independent memory structures; and the domain partitioning system is configured to include a first domain transaction routing process for routing transactions, which are received by said multi-port switch and specify the first domain, to one or more ports assigned to the first domain (figs. 1A and 1B and paragraph [0016], wherein the system has at least two domains, each with its own address space; each domain containing a collection of nodes coupled to routers for communication).

As for claim 30, the argument for claim 28 applies. Oi also shows a second domain transaction routing process for routing transactions, which are received by said multi-port switch and specify the second domain, to one or more ports assigned to the second domain (paragraphs [0008] and [0016-0022]).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 10,11, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oi in view of Sun, European Patent Application EP 0 848 327 A2 (previously applied).

As for claim 10, the argument above for claim 3 applies. Oi does not specifically show maintaining a coherency of a cache memory for the first domain, however the processing nodes in Oi do contain the processor-memory part of the system. Sun shows maintaining a coherency of a cache memory for the first domain (page 3, lines 35-50). It would have been obvious to one of ordinary skill in the art at the time of the invention to maintain cache coherency in the system of Oi as shown by Sun in order to improve memory performance.

As for claim 11, the argument for claim 10 applies. Sun shows that said maintaining the coherency includes: monitoring a caching of system memory by the nodes associated with the first domain; and informing the nodes requiring a cache update that content of the system

memory they have cached has changed (page 3 as noted above and inherent in cache coherency).

As for claim 19, the argument above for claim 13 applies. Oi does not specifically show a domain cache coherency process for monitoring the caching of system memory by the nodes associated with the first domain, and informing the nodes requiring a cache update that the content of the system memory they have cached has changed (page 3, lines 35-50). It would have been obvious to one of ordinary skill in the art at the time of the invention to maintain cache coherency in the system of Oi as shown by Sun in order to improve memory performance.

Response to Arguments

6. Applicant's arguments with respect to claims 1-30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Claims 9 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art does not show the use of broadcast transactions within the domain as claimed.

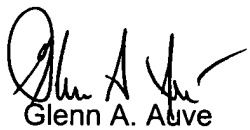
8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn A. Auve whose telephone number is (571) 272-3623. The examiner can normally be reached on M-F 8:00 AM-5:30 PM, every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Glenn A. Auve
Primary Examiner
Art Unit 2111

gaa
18 January 2005